REMARKS

Claims 1-60 are pending in the present application. Claims 12-29, 34-40, and 45-51 have been canceled in response to a restriction requirement. Various claims have been rejected under § 112 as being indefinite. All of the claims have been rejected under § 102(b) as being anticipated by Bland et al, US patent 5,703,537 (hereinafter "Bland") or under § 103 as being unpatentable over Bland in view of Kim, US patent 5,933,399 (hereinafter "Kim").

In the Specification

One paragraph of the Specification has been amended to include the patent number of a referenced patent application. No new matter has been added.

Section 112 Rejections

Claim 1

Claim 1 has been amended by replacing "providing" with "wherein" and adding "is provided" at line 5, and replacing "the" with "any" in line 6. Applicants believe that these amendments to claim 1 overcome the Examiner's rejections. The amendments to claim 1 described in this paragraph were not made to distinguish any prior art.

The Examiner has also stated that it is unclear how digital current can be created and reduced. To address the Examiner's question, please refer to the Specification, which states that:

> "The first technique attempts to reduce the digital current that causes spurs. Looking at the PLL circuitry 100 shown in Figure 1, a major source of digital current that causes interference is the divide-by-R counter 104. In a typical prior art PLL, such as that shown in Figure 1, the divide-by-R counter is implemented using a synchronous programmable counter. Synchronous programmable counters are readily designed and can easily be programmed to divide by a desired amount. One problem with synchronous programmable counters is that the counter will have a large number of components. Another problem with synchronous programmable counters is that every flip-flop in the counter is clocked at the same speed. The present invention reduces the digital current by reducing the number of components in the divide-by-R counter. This is accomplished by replacing the programmable counter by one or more fixed-value

counters and clocking at least one of the counters at a slower rate." Specification, page 14, lines 13-24.

The normal operation of a PLL causes "digital current". The present invention provides techniques for reducing the digital current, including "placing a fixed value divider at the input of the PLL", which reduces the number of components in the counter.

Claim 5

Claim 5 has been amended to delete "the" on line 2. This amendment to claim 5 was not made to distinguish the prior art.

With respect to the Examiner's other concerns, Applicants will refer to the Specification and drawings to address these concerns. The Examiner state that it is unclear what various recitations are and how various recitations read on the preferred embodiment.

An example of the method claimed in claim 5 is described in detail in the Specification from page 15, line 25 through page 18, line 15, and refers to Figure 5 (a block diagram) and Figure 6 (a schematic diagram of one example of a supply filter). As described in the Specification, mutual inductance exists between current loops in the digital circuitry in a PLL and current loops in a VCO. Briefly, one aspect of the invention functions as follows:

> "In digital circuitry (such as the digital circuitry comprising divide-by counters 204 and 205), a transmit loop is formed through the digital circuitry back to a supply, such as the voltage source that supplies voltage to the digital circuitry. Since the voltage source is located off the IC, the transmit loop can be relatively large. The present invention uses a supply filter (e.g., a low pass filter) to shorten the current loop, thereby reducing the mutual inductance between the digital circuitry of the PLL and the VCO." Specification, page 16, lines 6-11.

Referring to Figure 5, it can be seen that the current loop 332 (enabled by the filter 328) is smaller than current loop 330, which reduces the mutual inductance, since the mutual inductance relates to the size of the loops (such as loops 330 and 332).

Referring to the recitations in claim 5, Figure 5 shows an example of "digital circuitry", "filter", "area" (see loops 330 and 332), "voltage source", etc. Please note that Figure 5 shows just one example, and that other embodiments are possible.

Claims 8 and 9

With respect to claims 8 and 9, which depend from claim 5, the Examiner states that is not understood how the filter can confine currents. Referring to the discussion above, and to Figure 6, it can be seen that the filter 428 confines high frequency components of current (loops 436, 434) (see Specification, page 17, lines 15-17). Please note that Figure 6 shows just one example, and that other embodiments are possible.

Claim 30

The Examiner states that it is not understood what the "similar circuit elements" and "mirror images of one another" are, and how they can be "formed" and how this is read on the preferred embodiment. The technique claimed in claim 30 is a field cancellation technique, an example of which is described in detail in the Specification at page 22, lines 1-15, and illustrated in Figure 16. Referring to the described embodiment, in a circuit having a PLL and a VCO, for example, certain components of the PLL may induce a current in the VCO. For example, a flip-flop may induce an undesired current in the VCO. A similar circuit element (e.g., another flip-flop) would induce a similar current in the VCO. However, if one of the flip-flops is formed as a mirror image of the other (i.e., an opposite circuit layout), the fields created by the two flip-flops would tend to cancel each other out.

Claim 41

The Examiner states that it is unclear how the "circuitry" and "replica circuitry" can be "identified". Claim 41, and its dependent claims have been amended to help clarify the claims.

In claim 41, both steps have been replaced by a single step. Please note that claims 41-44 have not been amended to distinguish any prior art.

An example of a technique claimed in claim 41 is described in detail in the Specification at page 22, line 17 through page 25, line 4, and is shown in Figures 17-18. As stated in the Specification,

> "The next technique described addresses the problem of spurs caused by changes in impedance during the operation of a circuit. A change in impedance in a circuit occurs in portions of a circuit that change over time (see equation (12) above). For example, a flip-flop can change states (e.g., goes from high to low or low to high) during the operation of a circuit. When a flip-flop changes states, certain switching devices in the flip-flop are switched on or off. The switches that are turned on provide paths that define the geometry of various loops which, in turn, effects the inductance of the loops as well as the mutual inductance between loops. As was described above with respect to Figure 3, the frequency of oscillation of a VCO in the vicinity of a flip-flop will then vary with time, which results in spurs in the oscillator output spectrum." Specification, page 22, lines 17-26.
>
> "The present invention alleviates the problem described above by isolating portions of the digital circuitry that cause the spurs as a result of changing impedance and cancels the changing impedance by adding replica circuitry which operates in an opposite phase. The portions of the digital circuitry which are more likely to cause spurs include circuitry where a signal line runs over a relatively long route, because the mutual inductance M will have a large value for a larger route. In the example of an inverter, a replica inverter is created and is controlled to always be in the opposite phase as the original inverter. In this way, the impedance looking into the inverters is approximately constant independent of the state of the inverters because when one inverter is high, the other inverter will be low, and vise versa. The original and replica inverters and their routes should be matched and placed as close together as possible." Specification, page 23, lines 1-12.

Claim 52

In claim 52, the Examiner states that it is not understood what the "techniques" on line 5 are and how they can be "applied". The Specification describes in detail examples of various techniques to reduce interference. Any combination of techniques can be applied to achieve a desired result. In claim 52, a method is claimed for integrating VCO and PLL circuitry for a

wireless communication system onto a single IC. This type of integration is difficult, partly due to interference present near the frequency of the output of the VCO. By applying one or more of the techniques, this interference can be reduced.

Claim 53

See the discussion with respect to claim 1, above.

Claim 55

See the discussion with respect to claim 5, above.

Claim 56

An example of the technique claimed in claim 56 is described in the Specification at page 18, line 17 through page 21, line 25, and illustrated in Figures 8-15. The technique described reduces mutual inductance between current loops using conductive traces (e.g., see Figure 8).

Claim 57

See the discussion with respect to claim 30, above.

Claim 58

An example of the technique claimed in claim 58 is described in the Specification at page 25, line 6 through page 28, line 7, and illustrated in Figures 19-23. The technique described reduces mutual inductance between current loops by containing leakage current. The Specification describes buffer circuitry (e.g., 1782, 1784 in Figure 19), which is used to confine leakage current, which reduces the area of current loops, which reduces mutual inductance.

Claim 59

See the discussion with respect to claim 41, above.

Claim 60

An example of the technique claimed in claim 60 is described in the Specification at page 28, line 23 through page 29, line 14, and illustrated in Figures 24-25. The technique described addresses the problem of spurs caused by changes in impedance during the operation of a circuit. Figure 25 shows an RC filter inserted in an input line of an IC. By carefully selecting values for R3 and C3, the RC filter effectively isolates the impedance changes from the VCO but allows the desired signal to pass through.

Prior Art Rejections

Claims 1, 52-54, and 55-58 have been rejected under § 102 as being anticipated by Bland. Claims 2-11, 30-33, 41-44, and 59-60 have been rejected under § 103 as being unpatentable over Bland in view of Kim.

Claim 1

Claim 1 has been amended to incorporate the elements of canceled claim 2. Amended claim 1 claims a "method of reducing interference in a circuit having a PLL" ... comprising the steps of "providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount" and "wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL".

In rejecting claim 2, the Examiner states that Bland discloses a PLL circuit, but does not disclose that the divider (11) is comprised of a first and second divider. The Examiner then states that Kim teaches a circuit comprising a first divider (68) and a second divider (70) for providing a selectable divisor (Figure 6 of Kim). Amended claim 1 explicitly claims that the first

and second dividers are provided by placing first and second "fixed-value dividers", not selectable dividers, as taught by Kim.

It is therefore believed that amended claim 1 is not taught or suggested by the cited prior art. Since claims 3 and 4 depend from claim 1, it is also believed that they are not taught or suggested by the cited prior art.

Claim 5

Claim 5 claims a method of reducing interference comprising the step of "reducing mutual inductance between digital circuitry in a first portion of the circuit and circuitry in a second portion of the circuit by placing a filter between the digital circuitry and a voltage source external to the circuit in order to reduce the area of a high frequency current loop." Neither Bland nor Kim teach or suggest the method of claim 5. For example, neither reference teaches placing a filter between the digital circuitry and a voltage source to reduce the area of a current loop.

It is therefore believed that amended claim 5 is not taught or suggested by the cited prior art. Since claims 6-10 depend from claim 5, it is also believed that they are not taught or suggested by the cited prior art.

Claim 30

Claim 30 claims a method of reducing interference in a circuit "having a plurality of similar circuit elements" comprising the step of "forming at least some of the similar circuit elements on the circuit such that adjacent circuit elements are mirror images of one another." Neither Bland nor Kim teach or suggest the method of claim 30. For example, Bland and Kim do not teach forming similar circuit elements as mirror images of one another.

It is therefore believed that amended claim 30 is not taught or suggested by the cited prior art. Since claims 31-33 depend from claim 30, it is also believed that they are not taught or suggested by the cited prior art.

Claim 41

Claim 41 claims a method of reducing interference comprising the step of "creating replica circuitry of first circuitry in the circuit which has an impedance that changes state during operation of the circuit, wherein the replica circuitry operates in an opposite state relative to the first circuitry". Neither Bland nor Kim teach or suggest the method of claim 41. For example, Bland and Kim do not teach creating replica circuitry, or replica circuitry that operates in an opposite state of other circuitry.

It is therefore believed that amended claim 41 is not taught or suggested by the cited prior art. Since claims 42-44 depend from claim 41, it is also believed that they are not taught or suggested by the cited prior art.

Claim 52

Claim 52 claims a method of "integrating VCO and PLL circuitry for a wireless communication system onto a single integrated circuit" comprising the steps of "forming an integrated circuit having both PLL circuitry and VCO circuitry integrated on the integrated circuit" and "applying one or more techniques to reduce interference present near the frequency of an output of the VCO". Neither Bland nor Kim teach or suggest the method of claim 52. For example, Bland and Kim do not appear to suggest integrating VCO and PLL circuitry onto a single IC, or applying any techniques to reduce interference.

It is therefore believed that amended claim 52 is not taught or suggested by the cited prior art. Since claims 53-60 depend from claim 52, it is also believed that they are not taught or suggested by the cited prior art.

New Claims

New claims 61-65 have been added. Applicants submit that new claims 61-65 are not anticipated by the cited prior art.

Conclusion

It is respectfully submitted that all claims are patentable over the prior art. It is further more respectfully submitted that all other matters have been addressed and remedied and that the application is in form for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Bruce A. Johnson, Applicants' Attorney at 512-301-9900 so that such issues may be resolved as expeditiously as possible.

Respectfully Submitted,

2-3-03
Date

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PATENT TRADEMARK OFFICE

Replacement paragraphs, as amended:

(1) Page 30, first paragraph:

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The circuit shown in Figure 26 is described in detail in commonly owned, co-pending patent application serial number 09/087,485, filed on May 29, 1998, now US patent 6,327,463, and entitled "METHOD AND APPARATUS FOR GENERATING VARIABLE CAPACITANCE FOR SYNTHESIZING HIGH-FREQUENCY SIGNALS FOR WIRELESS COMMUNICATIONS", which is incorporated by reference herein.

Pending Claims, as amended:

1. A method of reducing interference in a circuit having a PLL, wherein the circuit is formed on an integrated circuit, the method comprising the steps of:

providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount; and

wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL.

3. The method of claim 2, wherein the one of the dividers divides the input frequency by thirteen and the other divider divides the input frequency by five.

4. The method of claim 1, wherein:

the PLL is powered by a first voltage;

the divider circuit is powered by a second voltage; and

the second voltage is less than the first voltage.

5. A method of reducing interference present in a circuit comprising the step of:

reducing mutual inductance between digital circuitry in a first portion of the circuit and circuitry in a second portion of the circuit by placing a filter between the digital circuitry and a voltage source external to the circuit in order to reduce the area of a high frequency current loop.

6. The method of claim 5, wherein the circuit is formed on an integrated circuit, and wherein the first portion of the circuit includes PLL digital circuitry and the second portion includes a VCO.

7. The method of claim 5, wherein the filter is a low pass filter.

8. The method of claim 5, wherein the filter creates a secondary current loop for confining current at a desired frequency in the secondary current loop.

9. The method of claim 8, wherein the filter creates a third current loop for confining current at a desired frequency in the third current loop.

10. The method of claim 5, wherein the filter is provided by placing a capacitor across first and second nodes in the digital circuitry and placing a resistor between the first node and the voltage source.

11. The method of claim 10, wherein the filter is further provided by placing a second capacitor between the second node and the resistor and placing a second resistor between the first resistor and the voltage source.

30. A method of reducing interference present in a circuit, the circuit having a plurality of similar circuit elements, the method comprising the step of:

forming at least some of the similar circuit elements on the circuit such that adjacent circuit elements are mirror images of one another.

31. The method of claim 30, wherein the circuit is formed on an integrated circuit having PLL and VCO circuitry for a wireless communications system.

32. The method of claim 30, wherein the circuit elements are flip flops.

33. The method of claim 32, wherein the flip flops form counters for the PLL.

41. A method of reducing interference present in a circuit formed on an integrated circuit having PLL and VCO circuitry, the method comprising the step of:

creating replica circuitry of first circuitry in the circuit which has an impedance that changes state during operation of the circuit, wherein the replica circuitry operates in an opposite state relative to the first circuitry.

42. The method of claim 41, wherein the replica circuitry has no function in the circuit other than reducing interference.

43. The method of claim 41, wherein the first circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the second inverter is controlled to be in the opposite state of the first inverter.

44. The method of claim 41, wherein the replica circuitry is comprised of circuitry similar to the first circuitry, the method further comprising the step of connecting an inverter between an input of the first circuitry and an input of the replica circuitry.

52. A method of integrating VCO and PLL circuitry for a wireless communication system onto a single integrated circuit comprising the steps of:

forming an integrated circuit having both PLL circuitry and VCO circuitry integrated on the integrated circuit; and

applying one or more techniques to reduce interference present near the frequency of an output of the VCO.

53. The method of claim 52, wherein the one or more techniques includes providing fixed divider circuitry for the PLL.

54. The method of claim 53, wherein the divider circuitry further comprises first and second series connected fixed dividers.

55. The method of claim 52, wherein the one or more techniques includes reducing the mutual inductance between digital circuitry in the PLL and the VCO circuitry by placing a filter between digital circuitry in the PLL and a voltage source external to the integrated circuit in order to reduce the area of a high frequency current loop.

56. The method of claim 52, wherein the one of the one or more techniques includes:

identifying a conductive trace on the integrated circuit carrying high frequency digital current; and

placing a conductive strip in the proximity of the identified conductive trace to help contain the high frequency digital current flowing through the conductive trace.

57. The method of claim 52, wherein the integrated circuit includes a plurality of similar circuit elements, and wherein one of the one or more techniques includes forming at least some of the similar circuit elements on the integrated circuit such that adjacent circuit elements are mirror images of one another.

58. The method of claim 52, wherein one of the one or more techniques includes providing a first block of digital circuitry connected to a second block of digital circuitry by a signal line, and inserting buffer circuitry between the first and second blocks of digital circuitry for containing high frequency current within the first block of digital circuitry.

59. The method of claim 52, wherein one of the one or more techniques includes the steps of: identifying circuitry in the integrated circuit in which the impedance of the circuitry changes over time during operation of the integrated circuit; and

creating replica circuitry of the identified circuitry which operates in a phase opposite of the identified circuitry.

60. The method of claim 52, wherein the integrated circuit includes an interface pin, wherein one of the one or more techniques includes the step of:

providing a filter coupled to the interface pin of the integrated circuit to reduce interference caused by signals at the interface pin.

61. A method of reducing interference present in a circuit formed on an integrated circuit, the method comprising the step of:

providing first circuitry in the circuit, wherein the first circuitry has an impedance that changes state during operation of the circuit; and

creating replica circuitry of the first circuitry, wherein the replica circuitry operates in an opposite state relative to the first circuitry.

62. The method of claim 61, wherein the replica circuitry has no function in the circuit other than reducing interference.

63. The method of claim 61, wherein the first circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the second inverter is controlled to be in the opposite state of the first inverter.

64. The method of claim 61, wherein the replica circuitry is comprised of circuitry similar to the first circuitry, the method further comprising the step of connecting an inverter between an input of the first circuitry and an input of the replica circuitry.

65. The method of claim 61, wherein the integrated circuit has PLL and VCO circuitry.